

67,200-261
Serial Number 09/821,521

Claim 9 is twice amended herein to correct a typographic omission.

Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 9-15 under 35 U.S.C. § 103(a) as being unpatentable over Jacobson et al. (U.S. Patent No. 6,294,401; hereinafter "Jacobson").

Applicant notes that the Examiner within the sentence bridging pages 2-3 of the Office communication mailed on 30 July 2002 and made FINAL acknowledges that Jacobson does not disclose a spirally patterned conductor layer having formed within its center a microelectronic structure comprising a series of at least four electrically interconnected sub-patterns. Applicant also notes that the Examiner nonetheless asserts that it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to modify the interconnected sub-patterns of Jacobson by adding more sub-patterns to provide applicant's claimed invention in order to form a microelectronic device having a desired function.

With respect to Jacobson, applicant notes that Jacobson (Fig. 4 and col. 7, lines 9-30) discloses that Jacobson's electronic identification tag is activated by a magnetic field from an external coil, preferably at a resonant frequency of an inductor and a pair of interconnected capacitors within Jacobson's electronic identification tag (i.e., Jacobson's inductor and pair of interconnected capacitors presumably serve as a resonant inductor-capacitor antenna circuit with respect to the magnetic field from the external coil). Within Jacobson's electronic identification tag, a separate logic module provides a time based digital response (i.e. signature) of Jacobson's

67,200-261
Serial Number 09/821,521

electronic identification tag to the external coil. Within the context of Jacobson's disclosure of operation of Jacobson's electronic identification tag, applicant is simply unable to discern any function within Jacobson's electronic identification tag which would be enhanced by further patterning of Jacobson's pair of interconnected capacitors within Jacobson's electronic identification tag, such as to provide a microelectronic fabrication in accord with applicant's microelectronic fabrication as disclosed and claimed within twice amended claim 9.

Thus, since: (1) the Examiner has predicated a suggestion or motivation for modification of Jacobson's electronic identification tag to provide applicant's microelectronic fabrication upon a suggestion or motivation within Jacobson to form a microelectronic device having a desired function; and (2) applicant is unable to locate within Jacobson any desired function which would be effected by modification of Jacobson's electronic identification tag to provide applicant's microelectronic fabrication, applicant asserts that twice amended claim 9 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Jacobson, for reasons as advanced by the Examiner.

Since claims 11-14 are dependent upon twice amended claim 9 and carry all of the limitations of twice amended claim 9, applicant additionally asserts that those claims may also not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Jacobson, for reasons as advanced by the Examiner.

67,200-261
Serial Number 09/821,521

In response in a second instance, applicant has added new claim 16 which is styled after twice amended claim 9 but incorporates therein an additional limitation which applicant believes to further explicitly address the Examiner's basis for rejection of applicant's claims 9-15 under 35 U.S.C. § 103(a) as being unpatentable over Jacobson. In conjunction with newly added claim 16, applicant has canceled claim 10.

In that regard, applicant has within newly added claim 16 explicitly incorporated therein the limitation that applicant's microelectronic structure formed within the center of applicant's spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns such as to attenuate eddy currents within the microelectronic structure. Support for this additional limitation explicitly incorporated into newly added claim 16 is found within applicant's specification within paragraph 0035.

Applicant further notes that Jacobson's electronic identification tag (Fig. 4 and col. 7, lines 9-30) which comprises an inductor and a pair of interconnected capacitors is unlikely to experience eddy currents in its static state since there is no indication that Jacobson's electronic identification tag is powered in its static state. In addition applicant again notes that Jacobson's electronic identification tag's response is a digital response activated by a magnetic field from an external coil and controlled by a separate logic circuit within Jacobson's electronic identification tag. Applicant is unable to locate within Jacobson any suggestion that eddy currents would actually occur incident to external magnetic field activation of Jacobson's

67,200-261
Serial Number 09/821,521

electronic identification tag or that additional patterning of Jacobson's pair of interconnected capacitors to effect eddy current attenuation would be a desired function within Jacobson's electronic identification tag.

Thus, since: (1) applicant's invention as disclosed and claimed within newly added claim 16 provides for a microelectronic fabrication comprising a spirally patterned conductor layer having formed within its center a microelectronic structure which comprises a series of at least four electrically interconnected sub-patterns which in turn serve the desired function of attenuating eddy currents within the microelectronic structure; (2) the Examiner has predicated suggestion or motivation for modification of Jacobson's electronic identification tag to provide applicant's microelectronic fabrication upon a need within Jacobson to form a microelectronic device having a desired function; and (3) applicant is unable to locate within Jacobson that applicant's desired function as claimed within newly added claim 16 is pertinent within Jacobson's electronic identification tag, applicant asserts that newly added claim 16 may not properly be rejected under 35 U.S.C. § 103(a) over Jacobson, for reasons as advanced by the Examiner.

In response in a third instance, applicant has amended claim 15 to incorporate therein all of the limitations from twice amended claim 9 from which it previously depended (absent the limitation of the series of at least four electrically interconnected sub-patterns), to thus provide an independent claim incorporating an additional limitation of a bond wire bonded upon applicant's microelectronic structure, wherein the bond wire has incorporated therein a minimum of one loop.

67,200-261
Serial Number 09/821,521

Applicant asserts that the foregoing limitation is clearly not present within Jacobson, nor would there be any suggestion or motivation for modification of Jacobson's electronic identification tag to provide applicant's invention in accord with applicant's amended claim 15, since Jacobson's electronic identification tag is activated by a magnetic field from an external coil and thus requires no apparent bond wire connection.

Thus, applicant asserts that amended claim 15 may not properly be rejected under 35 U.S.C. § 103(a) as being unpatentable over Jacobson.

In light of the foregoing responses applicant requests that the Examiner's rejections of applicant's claims 9-15 under 35 U.S.C. § 103(a) as being unpatentable over Jacobson be withdrawn.

Other Considerations

Applicant again acknowledges the prior art of record previously cited by the Examiner but not employed in rejecting applicant's claims to applicant's invention, including: (1) Staudinger et al. (U.S. Patent No. 5,416,356) and (2) Burghartz et al. (U.S. Patent No. 6,114,937), as generally pertinent to applicant's invention.

No fee is due as a result of this Amendment and Response.

67,200-261
Serial Number 09/821,521

SUMMARY

Applicant's invention as disclosed and claimed within twice amended claim 9, amended claim 15 and newly added claim 16 is directed towards a microelectronic fabrication, wherein the microelectronic fabrication comprises formed over a substrate a spirally patterned conductor layer. Within applicant's invention, the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer. Within applicant's invention, the spirally patterned conductor layer forms a planar spiral inductor, and the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of electrically interconnected sub-patterns (preferably at least four) to which may be bonded a bond wire having incorporated therein a minimum of one loop, such as to attenuate eddy currents within the microelectronic structure. Absent from the prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure of each and every limitation within applicant's invention as disclosed and claimed within amended claim 15 and newly added claim 16, nor is there and suggestion or motivation to modify the prior art of record to provide applicant's invention as disclosed and claimed within twice amended claim 9, amended claim 15 and newly added claim 16, for reasons as advanced by the Examiner.

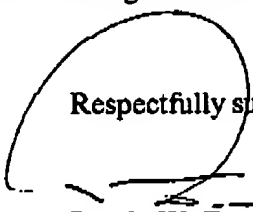
67,200-261
Serial Number 09/821,521

CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,



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67,200-261
Serial Number 09/821,521

APPENDIX
COMPLETE COPY OF THE CLAIMS
(MARKED-UP WITH CURRENT REVISIONS)

1. - 8. (canceled)

9. (twice amended) A microelectronic fabrication comprising:

a substrate; and

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns.

10. (canceled)

11. The microelectronic fabrication of claim 9 wherein the microelectronic structure is selected from the group consisting of resistors, diodes, capacitors, bond pads and aggregates thereof.

12. The microelectronic fabrication of claim 9 wherein the microelectronic structure comprises a capacitor electrically connected with a bond pad.

67,200-261
Serial Number 09/821,521

13. The microelectronic fabrication of claim 9 wherein the spirally patterned conductor layer is formed of a conductor material selected from the group consisting of non-magnetic metal, non-magnetic metal alloy, magnetic metal, magnetic metal alloy, doped polysilicon and polycide conductor materials, and laminates thereof.

14. The microelectronic fabrication of claim 9 wherein the spirally patterned conductor layer is formed in a geometric shape selected from the group consisting of a triangle, a square, a rectangle, a higher order polygon, an ellipse and a circle.

15. (amended) A microelectronic fabrication comprising:

a substrate;

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of electrically interconnected sub-patterns;
and

[The microelectronic fabrication of claim 9 further comprising] a bond wire bonded upon the microelectronic structure, wherein the bond wire has incorporated therein a minimum of one loop.

67,200-261

Serial Number 09/821,521

16. (newly added) A microelectronic fabrication comprising:

a substrate; and

a spirally patterned conductor layer formed over the substrate, wherein the spirally patterned conductor layer terminates in a microelectronic structure formed within the center of the spirally patterned conductor layer, wherein the spirally patterned conductor layer forms a planar spiral inductor, and wherein the microelectronic structure formed within the center of the spirally patterned conductor layer comprises a series of at least four electrically interconnected sub-patterns, such as to attenuate eddy currents within the microelectronic structure.